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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,474	08/27/2003	Arkadiy Morgenshtein	26327	5738

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,474	MORGENSHTEIN ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-18,20-46 and 55-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-18 and 20-32* is/are allowed.

6)☒ Claim(s) *1-3,5-15,33-35,37-46,55 and 56* is/are rejected.

7)☒ Claim(s) *4, 36, 57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 4, 2006 has been entered.

Claim Objections

Claims 1, 14, 15, 22-24, and 55 are objected to because of the following typographical errors:

Claim 1, line 8, the recitation, "said network" should be changed to "said p-type transistor network" and on line 17, the recitation, "said network" should be changed to "said n-type transistor network" in order to have proper antecedent basis.

Claims 14 and 15 should depend from either 1 or 8 or further limit the subject matter of a previous claim since depending claim 2 recites, "said first and second logic inputs are connected to form a first common logic input". With this limitation, the logic circuit cannot implement a ((NOT A) OR B) or ((NOT A) AND B) logic operation.

Claims 22-24 should depend from 16 or further limit the subject matter of a previous claim. The same reasoning applies as claims 14 and 15 stated above.

Claim 55, line 14, "4outer" appears to be "outer".

Claims 9, 10, 41, and 42 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is

required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Since the p-type transistor network already comprises a plurality of p-type transistors in independent claim, the p-type transistor network cannot comprise a single p-type transistor in dependent claim. The same reasoning applies to said n-type transistor network.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-15, 33-35, and 37-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Sako (US 6,084,437).

Regarding claim 1, Sako discloses, at least in figures 15-19, a complementary logic circuit, comprising:

a first logic input (c in Fig. 17);

a second logic input (/c);

a first dedicated logic terminal (a);

a second dedicated logic terminal (b);

a first logic block (M1B, M2B; D2 in Fig. 18) comprising:

a p-type transistor network (M1B, M2B) for implementing a predetermined logic function, said p-

type transistor network comprising a plurality of p-type transistors (M1B, M2B), and having an outer diffusion connection (A; see Fig. 18), a first network gate connection (G1; P in Fig. 18), and an inner diffusion connection (U), said outer diffusion connection of said p-type transistor network being connected to said first dedicated logic terminal (see "a" in Fig. 17), and said first network gate connection of said p-type transistor network being connected to said first logic input (c); and

a second logic block (M1A, M2A; D1 in Fig. 18) comprising:

an n-type transistor network (M1A, M2A) implementing logic function complementary to said predetermined logic function, said n-type transistor network comprising a plurality of n-type transistors (M1A, M2A), and having an outer diffusion connection (B), a first network gate connection (G2; Q in Fig. 18), and an inner diffusion connection (U),

said outer diffusion connection of said n-type transistor network being connected to said second dedicated logic terminal (see "b" in Fig. 17), and said first network gate connection of said n-type transistor network being connected to said second logic input (/c);

said inner diffusion connections of said p-type transistor network (12) and of said n-type transistor network (top portion of T1 in Fig. 8) being connected to form a common diffusion logic terminal (U).

Regarding claim 2, Sako discloses, at least in figure 17, that the first and second logic inputs are connected to form a first common logic input ("c" via an inverter such as I3 in Fig. 9; or see "c" in Fig. 15).

Regarding claim 3, Sako discloses, at least in figure 17, that each of said logic terminals is separately configurable to serve as a logic input (a, b).

Regarding claim 5, Sako discloses, at least in figure 16, a third logic input ("f" in T2) connected to a second network gate connection of said p-type transistor network (P in T2).

Regarding claims 6 and 7, Sako discloses, at least in figure 16, a fourth logic input (/f in

T2) connected to a second network gate connection of said n-type transistor network (Q in T2).

Regarding claim 8, Sako discloses, at least in figure 16, that said third and fourth logic inputs being connected to form a second common logic input ("f" via an inverter such as I2 in Fig. 9; or see "f" in Fig. 15).

Regarding claim 9, Sako discloses, at least in figure 15, that said p-type transistor network comprises a single p-type transistor (M2).

Regarding claim 10, Sako discloses, at least in figure 15, said n-type transistor network comprises a single n-type transistor (M1).

Regarding claim 11, Sako discloses that said p-type transistor network comprises one of a group of networks comprising: a network of p-type field effect transistors (FET) (col. 20, lines 46+), a network of p-type p-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type n-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type twin-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type silicon on insulator (SOI) transistors, and a network of p-type silicon on sapphire (SOS) transistors.

Regarding claim 12, Sako discloses, at least in figures 15-20, that said n-type transistor network comprises one of a group of networks comprising: a network of n-type FETs (col. 20, lines 46+), a network of n-type p-well CMOS transistors, a network of n-type n-well CMOS transistors, a network of n-type twin-well CMOS transistors, a network of n-type SOI transistors, and a network of n-type SOS transistors.

Regarding claim 13, Sako discloses that one of a group of logic circuits comprising: an OR gate, an inverted OR (NOR) gate, an AND gate, a multiplexer gate (see Figs. 15, 17 and 19), an inverter gate, and an exclusive OR (XOR) gate.

Regarding claim 14, Sako discloses that said logic circuit is operable to implement a ((NOT A) OR B) logic operation upon logic inputs A and B (e.g. see Fig. 25).

Regarding claim 15, Sako discloses that said logic circuit is operable to implement a ((NOT A) AND B) logic operation upon logic inputs A and B (e.g. see Figs. 15 or 16).

Claims 33-35 and 37-44 are essentially the same in scope as claims 1-3, 5-12 and are rejected similarly.

Regarding claim 45, Sako discloses, at least in figure 15, at least one buffer element (an inverted buffer I1 and I3).

Regarding claim 46, Sako discloses, at least in figure 15, at least one inverter (I1).

Claims 55 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Keeth (US 5,917,758).

Regarding claim 55, Keeth discloses, in figure 9A, a logic element comprising:

a first logic input (316);

a second logic input (305);

a first dedicated logic terminal (source terminal of 302);

a second dedicated logic terminal (source terminal of 304);

a p-type transistor (302), having an outer diffusion connection (source), a gate connection (gate), and an inner diffusion connection (drain); and

a n-type transistor (304), having an outer diffusion connection (source), a gate connection (gate), and an inner diffusion connection (drain);

said first logic input (316) being connected to said gate connection of said p-type transistor, said second logic input (305) being connected to said gate connection of said n-type transistor, said first dedicated logic terminal (source terminal of 302) being connected to said outer diffusion connection of said p-type transistor, said second dedicated logic terminal (source

terminal of 304) being connected to said outer diffusion connection of said n-type transistor, and said inner diffusion connection of said p-type transistor and said inner diffusion connection of said n-type transistor being connected to form a common diffusion logic terminal (306), said first and second logic inputs being configured as independent inputs (316, 305).

Regarding claim 56, Keeth discloses, in figure 9A, that wherein each of said logic terminals is separately configurable to serve as a logic input (col. 4, line 64 - col. 5, line 16).

Response to Arguments

Applicant's arguments with respect to claims 1-18, 20-46, and 55-57 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 16-18, and 20-32 are allowable over the prior art.

Claims 4, 36, and 57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER